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SYNCHRONIZED RECTIFYING CONTROLLER FOR A FORWARD POWER CONVERTER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a forward power converter. More particularly, the present invention relates to a synchronized rectifying controller for the forward power converter.

Description of the Related Art

Power converters are widely used in various electronic products to convert an AC input voltage into a DC supply voltage.

Various topologies such as flyback, forward, half-bridge, and full-bridge have been developed for different power needs. In traditional power converters, diodes are usually used as secondary rectifying components. In practical applications where high output currents frequently occur, the high forward voltage drop across the diodes causes significant power loss, which reduces power conversion efficiency. To avoid this problem, some power supplies use MOSFETs having low on-state resistance, instead of diodes. This substitution can reduce power consumption and improve power conversion efficiency.

Some synchronized rectifying controllers sense the primary gate signal to avoid cross-conduction from the secondary-side MOSFETs. This technique, however, can reduce propagation delay, but it requires an opto-coupler or an additional transformer to maintain isolation between the primary-side and the secondary-side of the transformer. This increases the cost and complexity of the circuit. Another drawback of this approach is that the circulated conduction losses increase under light-load condition. Such

reversed inductor currents increase component stress and reduce power conversion efficiency.

Therefore, a synchronized rectifying controller that features low system cost, high system efficiency and precise switching timing control is desired.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a synchronized rectifying controller to control the rectifying MOSFETs of the forward power converter.

It is another object of the present invention to prevent cross-conduction between the rectifying MOSFETs.

It is a further object of the present invention to prevent reverse inductor currents. This reduces component stress and improves power conversion efficiency under light-load conditions. The forward power converter according to the present invention includes a current-sense mechanism to avoid reverse currents from the output inductor.

It is another object of the present invention to detect the voltage from the secondary winding of the transformer. This reduces the cost and complexity of the detection circuit.

According to an aspect of the present invention, the synchronized rectifying controller prevents cross-conduction of the rectifying MOSFETs by controlling a maximum on-time of a second rectifying MOSFET, in a manner that is programmable and precise.

It is to be understood that both the foregoing general descriptions and the following detailed descriptions are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

FIG. **1** shows a schematic diagram of a traditional forward power converter using diodes as rectifying components;

FIG. **2A** shows the circuit operation of a traditional forward power converter while a primary-side MOSFET is turned on;

FIG. **2B** shows the circuit operation of a traditional forward power converter while the primary-side MOSFET is turned off;

FIG. **3** shows a schematic diagram of a traditional forward power converter using MOSFETs as rectifying components;

FIG. **4** shows a schematic diagram of a forward power converter applying a synchronized rectifying controller according to the present invention;

FIG. **5** shows a forward power converter applying the synchronized rectifying controller according to a preferred embodiment of the present invention;

FIG. **6** shows the synchronized rectifying controller according to a preferred embodiment of the present invention;

FIG. **7** shows a single-pulse generator of the synchronized rectifying controller according to a preferred embodiment of the present invention; and

FIG. **8** shows the timing diagram of the synchronized rectifying controller according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows a typical forward power converter. When a primary-side MOSFET **10** is turned on by a logic-high PWM signal, energy is transferred from a primary winding $\mathbf{N_P}$ to a secondary winding $\mathbf{N_S}$ of a transformer **11**. The primary winding $\mathbf{N_P}$ and the secondary winding $\mathbf{N_S}$ have same polarity. As FIG. **2A** shows, the voltage across the secondary winding $\mathbf{N_S}$ of the transformer **11** will start to charge an output inductor **17** and an output capacitor **14** via a rectifying diode **12**. Once the PWM signal drops to logic-low, as shown in FIG. **2B**, the primary-side MOSFET **10** will be turned off and the output inductor **17** will begin to release its energy to the output capacitor **14** via a rectifying diode **13**. However, the on-state voltage drop across the secondary-side rectifying diodes **12** and **13** causes significant power consumption, which reduces power conversion efficiency. In order to solve this problem, the secondary-side rectifying diodes are replaced with MOSFETs. The parasitic diodes of the MOSFETs have low on-state voltage drops, so this technique can improve power conversion efficiency.

As FIG. **3** shows, a parasitic diode **19** of a MOSFET **15** and a parasitic diode **18** of a MOSFET **16** respectively replace the rectifying diode **12** and the rectifying diode **13** shown in FIG. **1**. By properly synchronizing the gate signals of the MOSFETs **15** and **16**, the forward converter can produce the same output power while reducing power loss. To precisely synchronize the gate signals of the MOSFETs **15** and **16**, it is necessary to accurately detect the PWM signal.

FIG. **4** shows a schematic circuit diagram of a forward power converter having a synchronized rectifying controller **30** according to the present invention. Referring to FIG. **4**, the forward power converter comprises a transformer **11** having a primary winding $\mathbf{N_P}$ connected to a primary circuit and a secondary winding $\mathbf{N_S}$ connected to a

secondary circuit. A primary-side MOSFET **10** is coupled to the primary winding N_P of the transformer **11** to control power conduction. A detection diode **20** is connected between a positive end of the secondary winding N_S of the transformer **11** and a detection input **DET** of the synchronized rectifying controller **30**. An output inductor **17** is connected from the positive end of the secondary winding N_S of the transformer **11** and a positive output end of the power converter. An output capacitor **14** is connected across the positive output end of the power converter and the ground reference. A gate of a MOSFET **15** is driven by a first output **OUT1** of the synchronized rectifying controller **30**. A gate of a MOSFET **16** is driven by a second output **OUT2** of the synchronized rectifying controller **30**. A drain of the MOSFET **15** is connected to a negative end of the secondary winding N_S of the transformer **11**. A source of the MOSFET **15** is connected to a source of the MOSFET **16**. A drain of the MOSFET **16** is connected to the positive end of the secondary winding N_S of the transformer **11**. The source of the MOSFET **16** is connected to the ground reference via a current-sense mechanism **21**. The current-sense mechanism **21** is further coupled to the synchronized rectifying controller **30**.

The synchronized rectifying controller **30** has the detection input **DET** for detecting the PWM signal via detecting the voltage of the secondary winding N_S of the transformer **11**. Once a logic-high signal is detected at the detection input **DET** via the detection diode **20**, the synchronized rectifying controller **30** will turn on the MOSFET **15** and the energy from the secondary winding N_S will charge the output inductor **17** and the output capacitor **14** via the parasitic diode **19** of the MOSFET **15** during the conduction period. When the conduction period stops, the MOSFET **16** will be turned on and the energy stored in the output inductor **17** will be freewheeled into the output capacitor **14** via the parasitic diode **18** of the MOSFET **16**.

FIG. **5** shows the forward power converter according to one preferred

embodiment the present invention. The current-sense mechanism **21** shown in FIG. **4** is composed of a first resistor **80** and a second resistor **81**. The first resistor **80** is connected between the source of the MOSFET **16** and a positive-sense input **S+** of the synchronized rectifying controller **30**. The second resistor **81** is connected between the source of the MOSFET **16** and a negative-sense input **S-** of the synchronized rectifying controller **30**. The positive-sense input **S+** is connected to the ground reference of the power converter and a ground terminal **GND** of the synchronized rectifying controller **30**. A supply-voltage terminal **VCC** of the synchronized rectifying controller **30** is connected to the positive output end of the power converter. A timing resistor **31** is connected between a timing input **RT** of the synchronized rectifying controller **30** and the ground reference.

FIG. **6** shows the synchronized rectifying controller **30** according to a preferred embodiment of the present invention. The synchronized rectifying controller **30** comprises comparators **49, 50** and **51**, current sources **46, 47** and **48**, a NOT-gate **52**, an AND-gate **56**, an AND-gate **57**, two flip-flops **54** and **55** and a single-pulse generator **53**. A positive input of the comparator **49** and a negative input of the comparator **50** are coupled to the detection input **DET** of the synchronized rectifying controller **30**. The current source **48** is connected between the supply-voltage terminal **VCC** and the positive input of the comparator **49**. A reference voltage $\mathbf{V_{R1}}$ supplies a negative input of the comparator **49**. A reference voltage $\mathbf{V_{R2}}$ supplies a positive input of the comparator **50**. The current source **46** is connected from the supply-voltage terminal **VCC** to a negative input of the comparator **51**. The current source **47** is connected from the supply-voltage terminal **VCC** to a positive input of the comparator **51**. The positive input and the negative input of the comparator **51** are respectively the positive-sense input **S+** and the negative-sense input **S-** of the synchronized rectifying controller **30**. An output of the comparator **49** is connected to a first input $\mathbf{D_H}$ of the single-pulse

generator **53** and a CLOCK-input of the flip-flop **54**. A second input of the single-pulse generator **53** is coupled to the timing resistor **31**. An output of the single-pulse generator **53** is connected to a first input of the AND-gate **56** and a first input of the AND-gate **57**. An output of the comparator **50** is connected to a second input of the AND-gate **57**, an input of the NOT-gate **52**, and a CLOCK-input of the flip-flop **55**. An output of the flip-flop **55** is connected to a third input of the AND-gate **57**. An output of the comparator **51** is connected to a second input of the AND-gate **56**. The flip-flop **54** is reset by the output of the comparator **52** via the NOT-gate **52**. The flip-flop **55** is reset by an output of the AND-gate **56**. An input of the flip-flop **54** and an input of the flip-flop **55** are connected to the supply-voltage terminal **VCC**. The output of the flip-flop **54**, which is also the first output **OUT1** of the synchronized rectifying controller **30**, generates a first gate-signal to control the MOSFET **15** shown in FIG. **5**. The output of the AND-gate **57**, which is also the second output **OUT2** of the synchronized rectifying controller **30**, generates a second gate-signal to control the MOSFET **16** shown in FIG. **5**.

The transformer **11** is a forward transformer. When the PWM signal is logic-high, the primary-side MOSFET **10** will be turned on and the input voltage $\mathbf{V_{IN}}$ will be conducted through the primary winding $\mathbf{N_P}$ of the transformer **11**. The primary winding $\mathbf{N_P}$ and the secondary winding $\mathbf{N_S}$ of the transformer **11** will accumulate energy proportionally from the input voltage $\mathbf{V_{IN}}$. The voltage of the positive end of the secondary winding $\mathbf{N_S}$ will begin to rise. Eventually, it will exceed the voltage of the reference voltage $\mathbf{V_{R1}}$, causing the comparator **49** to output a logic-high signal. This logic-high signal generated by the comparator **49** will trigger the flip-flop **54**. The flip-flop **54** will then output a logic-high first gate-signal to the first output **OUT1** of the synchronized rectifying controller **30**.

When the PWM signal goes off, the voltage of the positive end of the secondary

winding N_S will drop to zero. The comparator **50** will output a logic-high signal to the input of the NOT-gate **52**. The NOT-gate **52** will invert this logic-high signal and reset the flip-flop **54** to clear the first gate-signal at the first output **OUT1** of the synchronized rectifying controller **30**.

When a level-high signal occurs at the positive end of the secondary winding N_S, the single-pulse generator **53** will be activated by the output of the comparator **49**. This will cause the single-pulse generator **53** to output a single-pulse signal S_O. The resistance of the timing resistor **31** determines a pulse width T_1 of the single-pulse signal S_O. When the voltage at the positive end of the secondary winding N_S drops below a level of a reference voltage V_{R2}, the flip-flop **55** will be triggered by the output of the comparator **50**. The flip-flop **55** will output a logic-high signal to the third input of the AND-gate **57**. When the output of the comparator **50**, the output of the flip-flop **55**, and the pulse-signal S_O are all logic-high, the AND-gate **57** will generate a logic-high second gate-signal to the second output **OUT2** of the synchronized rectifying controller **30**.

Following the period T_1, the single-pulse signal S_O will drop to logic-low and disable the AND-gate **57**. The output of the AND-gate **57** will be cleared to terminate the on-period of the second gate-signal. The pulse width T_1 introduces a delay time T_d before the start of the next switching signal. Without the delay time T_d, a short-circuit condition of the secondary winding N_S could occur as next switching cycle starts and the MOSFET **16** is still turned on. According to the present invention, the pulse width T_1 of the single-pulse generator **53** can be adjusted to determine a precise turn-off time of the MOSFET **16**. This ensures that the MOSFET **16** is turned off before next switching cycle starts.

FIG. **7** shows the single-pulse generator **53** according to a preferred embodiment of the present invention. The single-pulse generator **53** comprises an operational

amplifier (OPA) **60**, NOT-gates **69**, **70** and **71**, an AND-gate **72**, a MOSFET **62**, a current mirror composed of two MOSFETs **61** and **63**, current sources **64** and **65**, a capacitor **66**, a MOSFET **67** and a comparator **68**. A reference voltage V_{R3} is supplied to a positive input of the OPA **60**. A negative input of the OPA **60** is coupled to a source of the MOSFET **62** and the timing resistor **31**. An output of the OPA **60** is connected to a gate of the MOSFET **62**. A drain of the MOSFET **61**, a drain of the MOSFET **62**, a gate of the MOSFET **61**, and a gate of the MOSFET **63** are tied together. A source of the MOSFET **61** and a source of the MOSFET **63** are connected to the supply-voltage terminal **VCC**. A drain of the MOSFET **63** is connected to a negative input of the comparator **68** and a drain of the MOSFET **67**. The current source **64** is connected between the supply-voltage terminal **VCC** and the negative input of the comparator **68**. A reference voltage V_{R4} is supplied to a positive input of the comparator **68**. The capacitor **66** and the current source **65** are connected in parallel between the drain and a source of the MOSFET **67**. The source of the MOSFET **67** is connected to the ground reference. A gate of the MOSFET **67** is connected to an output of the AND-gate **72**. The NOT-gates **69**, **70** and **71** are connected in series. An output of the NOT-gate **69** is connected to an input of the NOT-gate **70**. An output of the NOT-gate **70** is connected to an input of the NOT-gate **71**. An output of the NOT-gate **71** is connected to a first input of the AND-gate **72**. A second input of the AND-gate **72** and an input of the NOT-gate **69** are connected to the output of the comparator **49** shown in FIG. **6**. An output of the comparator **68** is the output of the single-pulse generator **53**, which supplies the single-pulse signal S_O.

When the voltage at the positive end of the secondary winding N_S is low, the comparator **49** will output a logic-low signal to the first input D_H of the single-pulse generator **53**. This logic-low signal will disable the AND-gate **72**. The MOSFET **67** will remain off due to the logic-low signal output from the AND-gate **72**. The OPA **60**, the

MOSFET **62**, and the timing resistor **31** will generate a current $\mathbf{I_T}$. The current mirror mirrors the current $\mathbf{I_T}$ to a first current $\mathbf{I_1}$, which is coupled with the current source **64** to charge the capacitor **66**. The amplitude of the current $\mathbf{I_T}$ is given by following equation, where $\mathbf{R_T}$ is the resistance of the timing resistor **31**:

$$I_T = V_{R3} / R_T \qquad (1)$$

The first current $\mathbf{I_1}$ can be expressed by the following equation, where $\mathbf{N_{63}/\ N_{61}}$ is the geometric ratio of the MOSFETs **63** and **61**:

$$I_1 = (N_{63} / N_{61}) \times I_T \qquad (2)$$

Before the voltage across the capacitor **66** exceeds the voltage of the reference voltage $\mathbf{V_{R4}}$, which provides a threshold voltage for generating the single-pulse signal $\mathbf{S_O}$, the output of the single-pulse generator **53** will remain logic-high. The pulse width $\mathbf{T_1}$ of the single-pulse generator **53** is determined by the charge time of the capacitor **66**, which can be expressed by the following equation:

$$T_1 = \frac{C_{66} \times V_{R4}}{I_{64} + I_1 - I_{65}} \qquad (3)$$

Where $\mathbf{C_{66}}$ is the capacitance of the capacitor **66**, $\mathbf{I_{64}}$ is the current of the current source **64**, and $\mathbf{I_{65}}$ is the current of the current source **65**.

The current sources **64** and **65** are programmable. Increasing the current $\mathbf{I_{64}}$ and decreasing the current $\mathbf{I_{65}}$ can expand the delay time $\mathbf{T_d}$. Decreasing the current $\mathbf{I_{64}}$ and increasing the current $\mathbf{I_{65}}$ can shorten the delay time $\mathbf{T_d}$. This allows the delay time $\mathbf{T_d}$ to

be optimized to compensate for variations to the switching frequency. Such variations can be caused by factors such as temperature, component degradation, etc. The delay time $\mathbf{T_d}$ inserted before the start of each switching cycle can be expressed by the following equation:

$$T_d = T - T_1 \qquad (4)$$

Where **T** is the period of the PWM signal.

Once the voltage detected from the positive terminal of the secondary winding $\mathbf{N_S}$ exceeds the voltage of the reference voltage $\mathbf{V_{R1}}$, the voltage at the first input $\mathbf{D_H}$ of the single-pulse generator **53** will become logic-high. This logic-high signal will be supplied to the second input of the AND-gate **72**. However, the NOT-gates **69,70** and **71** will delay the signal from the first input $\mathbf{D_H}$ of the single-pulse generator **53**.

Before the logic-high signal from the first input $\mathbf{D_H}$ of the single-pulse generator **53** can propagate through to the first input of the AND-gate **72,** the output of the AND-gate **72** will be logic-high for an instant. This will turn on the MOSFET **67** to discharge the capacitor **66**. When the delayed signal from the first input $\mathbf{D_H}$ of the single-pulse generator **53** finally propagates through to the first input of the AND-gate **72**, the MOSFET **67** will be turned off. Then the capacitor **66** will begin to be charged.

Further referring to FIG. **5** and FIG. **6**, the resistors **80** and **81** are used to prevent an inverse discharge current flowing from the output capacitor **14** to the MOSFET **16**. When the capacitor **14** begins to supply an inverse discharge current, it will cause the voltage at the negative-sense input **S-** to exceed the voltage at the positive-sense input **S+**. The comparator **51** will output a logic-low signal to disable the output of the AND-gate **56**. This will reset the flip-flop **55** and turn off the second gate-signal at the second output **OUT2** of the synchronized rectifying controller **30**.

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It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the present invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided that they fall within the scope of the following claims and their equivalents.